Amendments to the Claims:

This listing of the claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1-7 (Canceled)

8 (New): A semiconductor device comprising:

a semiconductor substrate having two types of active regions that are a PMOS and an NMOS region separated from each other in plan view by a PN separation film;

a first gate electrode of P-type polycrystal silicon extending across said PMOS region and extending over said PN separation film;

first source and drain regions formed in said PMOS region at both sides of said first gate electrode;

a second gate electrode of N-type polycrstal silcon extending across said NMOS region and extending over said PN separation film;

second source and drain regions formed in said NMOS region at both sides of said second gate electrode;

a first insulating film formed over said first gate electrode in said PMOS region;

a second insulating film formed over said second gate electrode in said NMOS region;

a first sidewall insulating film formed on a side surface of said first gate electrode and said first insulating film;

a second sidewall insulating film formed on a side surface of said second gate electrode and said second insulating film;

a silicide film formed over said PN separation film and having a first side contacting said first gate electrode and a second side contacting said second gate electrode;

an interlayer insulating film formed over said first gate electrode, said first insulating film, and said first source and drain regions, and said interlayer insulating film having a contact hole overlapping one of said second source and drain regions and said second gate electrode in plan view; and

a conductive material filled in said contact hole and electrically connected to said one of second source and drain regions,

wherein said first and second sides of said silicide film are within said PN separation film in plan view and said first and second sides of said silicide film do not extend to said two types of active regions, and

wherein said interlayer insulating film covers a whole surface of said silicide film.

9 (New): A semiconductor device according to claim 8, wherein said first insulating film comprises a silicon nitride film and said interlayer insulating film comprises a silicon oxide film.

10 (New): A semiconductor device according to claim 8, wherein said first insulating film covers a whole top surface of said first electrode except a portion where said silicide film is formed.

11 (New): A semiconductor device according to claim 10, wherein said second insulating film covers a whole top surface of said second electrode except a portion where said silicide film is formed.

12 (New): A semiconductor device comprising:

a semiconductor substrate having two types of active regions that are a PMOS region and an NMOS region separated from each other in plan view by a PN separation film;

a first gate electrode of P-type polycrystal silicon extending across said PMOS region and extending over said PN separation film;

first source and drain regions formed in said PMOS region at both sides of said first gate electrode;

a second gate electrode of N-type polycrystal silicon extending across said NMOS region and extending over said PN separation film;

second source and drain regions formed in said NMOS region at both sides of said second gate electrode;

a first insulating film formed over said first gate electrode in said PMOS region;

a second insulating film formed over said second gate electrode in said NMOS region;

a first sidewall insulating film formed on a side surface of said first gate electrode and said first insulating film;

a second sidewall insulating film formed on a side surface of said second gate electrode and said second insulating film;

a silicide film formed over said PN separation film and having a first side contacting said first gate electrode and a second side contacting said second gate electrode;

an interlayer insulating film formed over said first gate electrode, said first insulating film, and said first source and drain regions, and said interlayer insulating film having a contact hole overlapping one of said second source and drain regions and said second sidewall insulating film in plan view; and

a conductive material filled in said contact hole and electrically connected to said one of second source and drain regions,

wherein said first and second sides of said silicide film are within said PN separation film in plan view and said first and second sides of said silicide film do not extend to said two types of active regions, and

wherein said interlayer insulating film covers a whole surface of said silicide film.

13 (New): A semiconductor device according to claim 12, wherein said first insulating film comprises a silicon nitride film and said interlayer insulating film comprises a silicon oxide film.

14 (New): A semiconductor device according to claim 12, wherein said first insulating film covers a whole top surface of said first electrode except a portion where said silicide film is formed.

15 (New): A semiconductor device according to claim 14, wherein said second insulating film covers a whole top surface of said second electrode except a portion where said silicide film is formed.